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10/633,701	08/05/2003	Mitsuhide Kato	36856.1102	6786

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,701	KATO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,7 and 13-15* is/are allowed.

6)☒ Claim(s) *2,5,6,8-12 and 17-21* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20060629*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed August 03, 2006. The Examiner acknowledges the amendments to Claims 2-9, 17, 18 and 20, and the cancellation of Claim 1. Accordingly, Claims 2-15 and 17-21 remain pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Van Dyke et al. (US 6,657,130 B2)† Chakravorty (US 6,970,362 B1)*

Ehman et al. (US 6,021,050)†

†Made of record by the Examiner in the Office Action of September 07, 2005.

*Made of record by the Examiner in the Office Action of March 06, 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 2, 5, 6, 8-11 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Dyke et al.

As to Claim 5, Van Dyke et al. discloses a laminated electronic component comprising: a laminated block (Figs. 2A-C) including a plurality of electrically insulating layers (33, 35, 37, 39) and an internal conductor film (patterned as stripes 36A,B,C,D; col.6: 61-65) disposed between the insulating layers (35 and 37) laminated together in a thickness direction of the laminated block; an external conductor film (patterned as stripes 32A,B,C,D; only 32B,C are shown in Figs. 2A-C; col.7: 45-48 and 63-65) disposed on an exposed (bottom) surface of the laminated block; and an additional conductor film (comprising stripes 34 A,B,C,D; col.7: 43-45 and 61-63) which is at the same electric potential (34B,D ground and 34A,C power) as the external conductor film (i.e., external film ground stripes 32A,C, corresponding to additional film ground stripes 34B,D; and external film power stripes 32 B,D, corresponding to additional film power stripes 34A,C (col.7: 43-48 and 61-65) and which is arranged along a specific interface between the insulating layers 33 and 35 (col.7: 43-45 and 61-63) such that the additional conductor film (34A,B,C,D in the Y-direction) faces--at the X-Y overlap regions--the external conductor film (32A,B,C,D in the X-direction) [*Examiner's Note*: although additional conductor film 34A,B,C,D is in the Y-direction, orthogonal to the external conductor film 32A,B,C,D in the X-direction, nevertheless additional conductor film 34A,B,C,D, located between insulating layers 33 and 35, *faces* external conductor film 32A,B,C,D, located at the bottom of insulating layer 33, *at the overlap region of X-Y intersection*, as can be clearly understood from Figs. 2A,B and col.7: 43-53 and 61-65]; wherein the insulating layers are formed of ceramic material (col.7: 35-37); the area of additional conductor film (stripes 34A,B,C,D) is greater than or equivalent to the area of

the external conductor film (stripes 32A,B,C,D), and is arranged such that the additional conductor film 34A,B,C,D covers--i.e., overlaps at the X-Y intersection of the overlapping stripes--the external conductor film 32A,B,C,D therein when viewed from above or below [*Examiner's Note*: This is best seen and understood from: (i) Figs. 2A-C; (ii) col.9: 51-58, which discloses that the prior art teaches the power and ground mesh planes, formed by the above-referenced power and ground stripes, respectively, each comprise 40% metal per layer; and (iii) col.10: 54-59 which discloses the modification of the prior art represented by Figs. 2A-C, wherein the metal loading is uniform for all of the layers, at about 25% to 30% metal per layer. Thus, Figs. 2A-C do fairly represent that the area of the additional conductor film (stripes 34A,B,C,D) is, at the very least, ***equivalent*** to the area of the external conductor film (stripes 32A,B,C,D), by virtue of the support for this rendering of the metallization in Figs. 2A-C provided in col.10: 54-59 of the disclosure]; and the external conductor film (bottom layer 33 of laminated component 30 in Figs. 2B,C--col.7: 63-65--comprising stripes 32A,B,C,D and ends of vias 40A,B,C,D and 42A,B,C,D) defines a land for mounting (shown in the bottom layer of component 30, in Fig. 3C and col.8: 37-54, where the bottom layer L10 is labeled BSM--bottom surface metallization--to which are attached the balls of the BGA on said lands for mounting, as shown in the plan view of L10 in Fig. 17 and referenced in col.13: 21-27).

As to Claim 2, Van Dyke et al. further discloses only one of the insulating layers (i.e., layer 33) is interposed between additional conductor film 34A,B,C,D and external conductor film 32A,B,C,D (Fig. 2B,C).

As to Claim 6, Van Dyke et al. further discloses that the additional conductor film patterned as 34A,B,C,D and the external conductor film patterned as 32A,B,C,D are (variously) electrically connected to each other through a via-hole conductor 42A,B,C,D and 40A,B,C,D (i.e., said via-hole conductor respectively connecting additional conductor film stripe patterns 34A,B,C,D to corresponding external conductor film stripe patterns 32A,B,C,D; Figs. 2A-C and col.7: 35-65).

As to Claim 8, Van Dyke et al. further discloses a DC bias is applied between the external conductor film and the internal conductor film such that the DC bias occurs between the external conductor film stripes 32B,D and the internal conductor film stripes 34A,C (Fig. 2C; col.7: 54-65).

As to Claim 9, Van Dyke et al. further discloses a first main (top) surface and a second main (bottom) surface facing the first main surface, and the external conductor film 32A,B,C,D is disposed on the second main surface.

As to Claim 10, Van Dyke et al. further discloses a chip component mounted on the first main (top) surface, wherein the external conductor film (comprising stripes 32A,B,C,D) is arranged to be in electrical connection with the vertical vias 40A,B,C,D and 42A,B,C,D which, in turn, establishes an electrical connection with the chip component by way of the conductive film layers above the external conductor film comprising stripes 32A,B,C,D (Fig. 7 and col.7: 48-53 and col.10: 60-col.11: 9; also, cols. 11-13 provide the details of each layer that connects with the one above it, by way of the vertical vias, to establish the connection between the external conductor film and the chip component).

As to Claim 11, Van Dyke et al. further discloses the chip component is one of an IC chip and a capacitor (Fig. 7; col.10: 60-65).

As to Claim 17, Van Dyke et al. further discloses internal conductor film (patterned as stripes 36A,B,C,D; Figs. 2A-C; col.6: 61-65) defines at least one of a ground potential and a wiring for connection to an electronic component, i.e., the chip mounted on the carrier surface (Figs. 2A-C and 7; col.11: 10-19).

As to Claim 18, Van Dyke et al. further discloses a plurality of internal conductors (L2-L16 in Figs. 8-16, respectively) and via-hole conductors (40A-D, 42A-D, as shown in Figs. 2A-C) which are arranged to provide wiring patterns (col.7: 48-53; Figs. 2A-C and the plurality of internal layers L1-L16 shown in Figs. 8-16, respectively).

As to Claim 19, Van Dyke et al. further discloses the plurality of internal conductors and via holes conductors are disposed in the laminated block (Figs. 2B,C and 8-16; col.7: 48-53).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Dyke et al. in view of Chakravorty.

I. Van Dyke et al. discloses a chip carrier (Figs. 2A-C and 7; col.11: 10-14), wherein it is old and well-known in the art that chip carriers are typically mounted to system circuit boards-- in this case, through the bottom surface ball grid array (BGA) metallurgy (layer L10 in Fig. 17 and col.13: 26-27) that carries the signals, power and ground to/from the system board and thereby provides the system with the functional electronics of the chip package. Van Dyke et al. does not depict or discuss a system board on which the laminated electronic component is mounted and to which the laminated electronic component is electrically connected.

II. Chakravorty provides evidence of this old and well-known application of the chip carrier in Fig. 2, wherein the chip carrier 50 is mounted and electrically connected to the system board 60 by the BGA metallurgy carrying signals, power and ground to the IC chip 40.

III. Since both Van Dyke et al. and Chakravorty teach the fabrication of carriers for packaging chips, and since Chakravorty shows the chip carrier mounted to a system circuit board to provide the board with the chip package functionality, then the mounting

of the chip carrier to a system board for providing the chip package functionality to the electronic system would have been readily recognized as an application of the chip carrier package in the pertinent art of Van Dyke et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the BGA chip carrier package of Van Dyke et al. to a system circuit board to impart the functional electronics of the chip, as enhanced by the package wiring, to the electronic system of the circuit board, as taught by Chakravorty.

8. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Dyke et al. in view of Ehman et al.

As to Claims 20 and 21:

I. Van Dyke et al. discloses a laminated block comprising a multilayer chip carrier with wiring arranged for optimizing electrical performance and requiring fewer layers (col.3: 21-34) and including discrete noise decoupling capacitors for protecting the chip (col.11: 10-19; col.12: 11-18). Van Dyke et al. does not teach resistor films for defining resistors disposed within the laminated block.

II. Ehman et al. discloses a laminated block 10 comprising a multilayer multi-component circuit board having chips 58 and discrete capacitors 60 mounted thereon, the laminated block 10 further including resistor films disposed on and within the laminated block 10 such that the cost and space required on the laminate block 10 is reduced by including some of said resistor films within the laminated block 10 (Fig. 1; col.1: 12-18 and 42-47; col.3: 13-25 and 46-53), the resistor films, in conjunction with

other printed and discrete passive elements, functioning as current limiters and as part of digital attenuators and terminating circuits (col.1: 25-28) in order to optimize electrical performance.

III. Since both Van Dyke et al. and Ehman et al. disclose a laminated block whose multilayered structure provides circuitry and components disposed thereon for optimizing electrical performance of the electronic elements, such as IC chips, and since both are concerned with reducing package size by reducing the package profile (less layers in Van Dyke et al., flatter components provided by printing techniques in Ehman et al.), then the additional employment of resistor films for the purpose of performing required circuit functions and signal conditioning with minimal addition to the laminate block profile, as taught by Ehman et al., would have been readily recognized for the same purpose in the laminate block carrier of the pertinent art of Van Dyke et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the laminate block of Van Dyke et al. by adding resistor functionality in the form of resistor films disposed within the laminated block in circuits requiring resistor functions, in order to optimize the electrical performance of the circuitry, and to effect such a high density of circuitry in the laminate block of Van Dyke et al. with minimal increase in the package profile, as taught by Ehman et al.

Allowable Subject Matter

9. Claims 4, 7 and 13-15 have been allowed.

10. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments, see pp.8-9 of the instant Amendment, filed August 03, 2006, with respect to Claim 5 as rejected under 35 USC § 102(e) over Chakravorty (US 6970362) have been fully considered and are persuasive. The rejection of Claim 5 under 35 USC § 102(e) over Chakravorty has been withdrawn.

12. Applicant's arguments on pp.8-9 of the instant Amendment, filed August 03, 2006, with respect to Claim 5 as rejected under 35 USC § 102(e) over Van Dyke et al. have been fully considered but they are not persuasive.

(a) Applicant argued that the Examiner relied on Fig. 2A to read on the limitation in Claim 5 that states "the area of said additional conductor film is greater than or equivalent to the area of said external conductor film, and is arranged such that said additional conductor film covers said external conductor film therein when viewed from above or below" and that no area dimensions are taught or fairly suggested in the disclosure, and therefore the cited case law--*Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956, 55 USPQ2d 1487, 1491 (Fed. Cir. 2000)--prohibits the

Examiner from using the Fig. 2A to teach or fairly suggest the equivalence of the respective areas of the external and additional conductor films, absent any disclosure in the Specification of such area dimensions.

(b) However, Van Dyke et al. is **not** "completely silent with respect to the dimensions (i.e., the areas) of the external conductor film and the additional conductor film," as the Applicant alleges on p.9, first full paragraph, of the above-cited Amendment arguments. As pointed out in the Examiner's rejection set forth above, Van Dyke et al. does, in fact, explicitly disclose that each of the laminated component layers, inclusive of the additional conductor film (Figs. 2A,B,C; stripes 34A,B,C,D at the base of layer 35) and the external conductor film (Figs. 2A,B,C; stripes 32A,B,C,D at the base of bottom layer 33) are uniformly metal-loaded at about 25% to 30% metal per layer which, with specific regard to the additional and external conductor films, implies that the area defined by the additional conductor film of layer 35 is, at the very least, equivalent to the area defined by the external conductor film of bottom layer 33, and the layout of the additional and external conductor films, as seen from above or below (Fig. 2A) is shown to be a mesh structure "arranged such that the additional conductor film covers the external conductor film therein when viewed from above and below," as explained by the Examiner in the rejection of Claim 5 set forth above. The area dimensions of the additional and external conductor films shown in Figs. 2A,B,C of Van Dyke et al. finds its explicit support in col.9: 51-58 in conjunction with col.10: 54-59, and the "covering" limitation (i.e., overlapping of the X-Y strips in the power and ground meshes in layers 35 and 33 shown in Figs. 2A,B,C, as explained in detail in the Examiner's rejection of

Claim 5, above) finds its explicit support in col.7: 43-53 and 61-65. Accordingly, the Examiner has maintained and repeated the rejections of Claims 2, 5, 6, 8-11 and 17-19 over Van Dyke et al. under 35 USC § 102(e), and the 35 USC § 103(a) rejections of Claim 12 (over Van Dyke et al. in view of Chakravorty) and Claims 20 and 21 (over Van Dyke et al. in view of Ehman et al.).

13. The new limitation added to Claim 5--i.e., "the external conductor film defines one of a die bonding surface and a land for mounting"--has been rejected over Van Dyke et al. in the Examiner's rejection of Claim 5 set forth above.

Conclusion

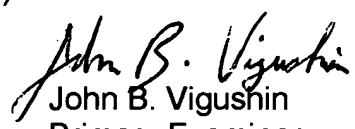
14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
October 11, 2006